19-4018; Rev 0; 3/06

MAX1217/MAX1218/MAX1219 Evaluation Kits

General Description

The MAX1217/MAX1218/MAX1219 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of the MAX1217/MAX1218/MAX1219 dual, 12-bit, 125Msps/170Msps/210Msps analog-to-digital converters (ADCs). These ADCs accept differential analog inputs, which the EV kit generates from user-provided single-ended input sources. The digital outputs produced by the ADC can be easily sampled using a high-speed logic analyzer or data-acquisition system. The EV kit operates from 1.8V/3.3V power supplies and includes circuitry that generates a differential clock signal from a single-ended AC source provided by the user.

Features

- **ADC Sampling Rates from 125Msps to 210Msps**
- **Low Voltage and Power Operation**
- **On-Board Clock-Shaping Circuitry**
- **On-Board LVDS/LVPECL Differential Level Translators**
- **Fully Assembled and Tested**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1217EVKIT	0°C to +70°C	100 TQFP-EP
MAX1218EVKIT	0°C to +70°C	100 TQFP-EP
MAX1219EVKIT	0°C to +70°C	100 TQFP-EP

EV Kit Specific Component List

EV KIT PART NUMBER	DESIGNATION	DESCRIPTION
MAX1217EVKIT	U1	Maxim MAX1217ECQ (100-pin TQFP)
MAX1218EVKIT		Maxim MAX1218ECQ (100-pin TQFP)
MAX1219EVKIT		Maxim MAX1219ECQ (100-pin TQFP)

Part Selection Table

PART	SPEED (Msps)
MAX1219ECQ	210
MAX1218ECQ	170
MAX1217ECQ	125

Common Component List

DESIGNATION	QTY	DESCRIPTION
C1, C3, C5, C6, C12, C13, C18, C42, C43	9	0.1µF ±20%, 25V X7R ceramic capacitors (0603) TDK C1608X7R1E104M
C2, C4, C115–C123	11	0.1µF ±20%, 6.3V X5R ceramic capacitors (0201) TDK C0603X5R0J104M
C7, C19, C20, C33–C41, C112, C113, C114	15	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M
C14–C17	4	2.0pF ±0.25pF, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H2R0C
C21–C32, C108–C111	16	0.01µF ±5%, 25V C0G ceramic capacitors (0603) TDK C1608C0G1E103J
C44–C70	27	0.01µF ±10%, 25V X7R ceramic capacitors (0402) TDK C1005X7R1E103K
C71–C74	4	220µF ±20%, 6.3V tantalum capacitors (C-case) AVX TPSC227M006R0250
C76–C79	0	Not installed (C-case)
C81–C84	4	10µF ±20%, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J106M
C86–C89, C91–C103	17	1.0µF ±20%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J105M
C104–C107	4	4.7µF ±20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J475M
J1, J3, J7, J15	4	SMA PC mount connectors
J5, J6, J14	3	2-pin headers
J8, J10, J11, J13	4	Dual-row, 50-pin headers
J9, J12	2	Dual-row, 6-pin headers
J16, J18	2	Triple-row, 75-pin headers
J17	1	Triple-row, 9-pin header
JU1, JU2	2	Jumpers, dual-row, 8-pin headers

Common Component List (continued)

DESIGNATION	QTY	DESCRIPTION
JU3–JU8	6	Jumpers, 3-pin headers
R1, R3, R23–R26, R121, R148, R151, R152	10	49.9Ω ±1% resistors (0603)
R2, R4, R5–R10, R13–R18, R112, R113, R150	0	Not installed (0603)
R19–R22	4	24.9Ω ±0.1% resistors (0603) Vishay/Dale TNPW060324R9BEEA IRC PFC-W0603R-02-24R9-B
R27–R107	81	49.9Ω ±1% resistors (0402)
R108–R111	4	10Ω ±0.1% resistors (0603) Vishay/Dale TNPW060310R0BEEA
R114	1	4.02kΩ ±1% resistor (0603)
R115	1	2kΩ ±1% resistor (0603)
R116	1	5kΩ potentiometer, 19-turn, 3/8in
R117, R118	2	13.0kΩ ±1% resistors (0603)
R119, R120	2	100kΩ potentiometers, 19-turn, 3/8in
R122–R147, R153	27	100Ω ±1% resistors (0603)
R149, R156	2	510Ω ±5% resistors (0603)
R154, R155	0	Not installed (T93YB)
T1–T4	4	1:1, 800MHz RF transformers Mini-Circuits ADT1-1WT
TP1–TP6	6	Test points (black)
U1	1	**Note:** See the *EV Kit Specific Component List*
U2	1	Maxim MAX9388EUP (20-pin TSSOP)
U3–U9	7	3.3V, ECL, quad differential receivers (SO-20) On Semiconductor MC100LVEL17DW
Y1	0	Not installed (VF561E)
—	8	Shunts
—	1	MAX1217/MAX1218/MAX1219 PC board

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
IRC	361-992-7900	361-992-3377	www.irctt.com
Mini-Circuits	718-934-4500	718-332-4661	www.minicircuits.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Vishay	402-564-3131	402-563-6296	www.vishay.com

Note: *Indicate that you are using the MAX1217/MAX1218/MAX1219 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Analog (AVCC) 1.8V, 1A
  - Output drive (OVCC) 1.8V, 250mA
  - Clock (VCLK) 3.3V, 100mA
  - Buffer (VPECL) 3.3V, 1A
- Signal generator with low phase noise and low jitter for clock input (e.g., HP/Agilent 8644B)
- Two signal generators for analog signal inputs (e.g., HP/Agilent 8644B)
- Logic analyzer or data-acquisition system (e.g., HP/Agilent 16500C, TLA621)
- Analog bandpass filters (e.g., Allen Avionics, K&L Microwave) for input signal and clock signal
- Digital voltmeter

Procedure

The MAX1217/MAX1218/MAX1219 EV kits are fully assembled and tested surface-mount boards. Follow the steps below for board operation. **Do not turn on power supplies or enable function generators until all connections are completed.**

1) Verify that shunts are installed in the following locations:

   JU1 (3-4) → Internal reference enabled (channel A)

   JU2 (3-4) → Internal reference enabled (channel B)

   JU3 (2-3) → Channel A output in two's-complement format

JU4 (2-3) → Channel B output in two's-complement format

JU5 (1-2) → Divide-by-two clock disabled

JU6, JU7 (2-3) → Variable duty-cycle input selected

2) Connect a 1.8V, 1A power supply to AVCC. Connect the ground terminal of this supply to GND.
3) Connect a 1.8V, 250mA power supply to OVCC. Connect the ground terminal of this supply to GND.
4) Connect a 3.3V, 100mA power supply to VCLK. Connect the ground terminal of this supply to GND.
5) Connect a 3.3V, 1A power supply to VPECL. Connect the ground terminal of this supply to GND.
6) Connect the clock signal generator to the input of the clock bandpass filter.
7) Connect the output of the clock bandpass filter to the EV kit SMA connector labeled J7. Monitor the clock signal using a differential oscilloscope probe at connector J14.
8) Connect the first analog signal generator to the input of the desired bandpass filter.
9) Connect the output of the first bandpass filter to the EV kit SMA connector labeled J1.
10) Connect the second analog signal generator to the input of the desired bandpass filter.
11) Connect the output of the second bandpass filter to the EV kit SMA connector labeled J3.
12) Ensure that all signal generators are phase-locked to a common reference frequency.
13) Connect the logic analyzer to either headers J8 to J10 (LVDS-compatible signals), J11 to J13 (LVPECL-compatible signals), or J16 to J18 (single-ended capture). See the *Output Bit Locations* section for header descriptions and connections.
14) Turn on all the power supplies.
15) With a voltmeter, verify that 1.32V is measured across test points TP3 and TP4. If the voltage is not 1.32V, adjust potentiometer R116 until 1.32V is obtained.
16) Enable the function generators.
17) Set the clock signal generator to output a 210MHz signal. The amplitude of the generator should be sufficient to produce a 13.8dBm (1.09V_{P-P}) signal at the SMA input of the EV kit. Insertion losses due to the series-connected filter (step 7) and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude.
18) Set the analog input signal generators to output the desired test frequency. The amplitude of the generator should produce a signal that is no larger than 11dBm (793mV_{P-P}) as measured at the SMA input of the EV kit. Insertion losses due to the series-connected filter (steps 8 and 10) and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude.
19) Enable the logic analyzer.
20) Collect data using the logic analyzer.

Detailed Description

The MAX1217/MAX1218/MAX1219 EV kits are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of the MAX1217/MAX1218/MAX1219 dual, 12-bit parallel output ADCs.

The MAX1217/MAX1218/MAX1219 accept differential inputs; however, on-board transformers (T1, T3) convert readily available single-ended source outputs to the required differential signals. Measure the inputs of the MAX1217/MAX1218/MAX1219 at headers J5 and J6 using a differential oscilloscope probe.

Output level translators (U3–U8) buffer and convert the LVDS output signals of the MAX1217/MAX1218/MAX1219 to higher-voltage LVPECL signals, which can be captured by a wide variety of logic analyzers. The LVDS outputs are accessed at headers J8, J9, J10. The LVPECL outputs are accessed at headers J11, J12, J13. Additionally, the LVPECL outputs can be captured with a single-ended logic-analyzer probe at headers J16, J17, and J18.

The EV kit is designed as a four-layer PC board to optimize the performance of the MAX1217/MAX1218/MAX1219. Separate analog, digital, clock, and buffer power planes minimize noise coupling between analog and digital signals. 50Ω coplanar transmission lines are used for analog and clock inputs. 100Ω-differential coplanar transmission lines are used for all digital LVDS outputs. All differential outputs are properly terminated with 100Ω termination resistors between true and complementary digital outputs. The trace lengths of the 100Ω-differential LVDS lines are matched to within a few thousandths of an inch to minimize layout-dependent data skew.

Power Supplies

The MAX1217/MAX1218/MAX1219 EV kits require separate analog, output-drive, clock, and buffer power supplies for best performance. Two 1.8V power supplies are used to power the analog (AVCC) and output-driver (OVCC) circuitry of the MAX1217/MAX1218/

MAX1219. The clock circuitry (VCLK) is powered by a 3.3V power supply. A separate 3.3V power supply (VPECL) is used to power the output buffers (U3–U9) of the EV kit.

Clock

The MAX1217/MAX1218/MAX1219 EV kits feature a variety of clock input methods. A differential clock signal can be generated from a single-ended sine wave applied to J15. A variable-duty-cycle differential clock signal can be generated from a single-ended sine wave applied to J7 (see the *Variable-Duty-Cycle Clock-Shaping Circuit* section). Alternatively, the on-board crystal oscillator can be utilized instead of a user-provided signal source (see the *On-Board Crystal Oscillator* section). U2 multiplexes all three of these inputs onto the MAX1217/MAX1218/MAX1219 clock input lines. Jumpers JU6 and JU7 control the multiplexer. See Table 1 for shunt settings.

Table 1. Clock Multiplexer Shunt Settings (JU6, JU7)

	JUMPER		DESCRIPTION
	JU6	JU7	
SHUNT POSITION	2-3*	2-3*	Variable-duty-cycle clock selected. Apply a signal to J7. Measure the duty cycle at J14.
	1-2	1-2	Differential clock signal selected. Apply a signal to J15.
	2-3	1-2	Clock disabled.
	1-2	2-3	On-board crystal oscillator selected. Enable crystal using JU8.

**Default configuration: JU6 (2-3), JU7 (2-3).*

Divide-by-Two Clock

The MAX1217/MAX1218/MAX1219 feature internal divide-by-two clock circuitry. Jumper JU5 controls this function. See Table 2 for shunt settings.

Table 2. Divide-by-Two Shunt Settings (JU5)

SHUNT POSITION	MAX1217/ MAX1218/MAX1219 CLKDIV PIN	DESCRIPTION
1-2*	AVCC	Clock signal is divided by 1.
2-3	GND	Clock signal is divided by 2.

**Default configuration: JU5 (1-2).*

On-Board Crystal Oscillator

To facilitate easy evaluation, the MAX1217/MAX1218/MAX1219 EV kits feature an open location for an on-board crystal oscillator. To use this function, install a three-pin header at location JU8. Also, install a crystal oscillator with the desired frequency at location Y1.

Jumper JU8 controls the enable function of the oscillator. See Table 3 for shunt settings. To improve performance of the EV kit, disable the crystal oscillator when not in use.

Table 3. Crystal Oscillator Shunt Settings (JU8)

SHUNT POSITION	DESCRIPTION
1-2	Crystal oscillator enabled.
2-3*	Crystal oscillator disabled.

**Default configuration: JU8 (2-3).*

Variable-Duty-Cycle Clock-Shaping Circuit

A differential multiplexer (U2) processes the single-ended sine wave (applied at J7) and generates the required differential clock signal. The clock signal's duty cycle can be adjusted with potentiometer R116. A clock signal with a 50% duty cycle (recommended setting) can be achieved by adjusting R116 until 1.32V is produced across test points TP3 and TP4 when the clock voltage supply (VCLK) is set to 3.3V. Measure the clock signal with a differential oscilloscope probe at J14.

Input Signal

The MAX1217/MAX1218/MAX1219 accept differential analog input signals; however, the EV kits only require a single-ended analog input signal, with an amplitude of less than 11dBm (793mV$_{P-P}$) provided by the user. On-board transformers (T1, T3) convert the single-ended analog inputs and generate differential analog signals at the ADC's differential input pins.

Reference Voltage

There are three methods to set the full-scale range of the MAX1217/MAX1218/MAX1219. The EV kits can be configured to use the MAX1217/MAX1218/MAX1219's internal reference, a stable low-noise external reference, or the on-board reference adjustment circuitry.

The MAX1217/MAX1218/MAX1219 feature an internal 1.23V bandgap reference circuit, which, in combination with an internal reference-scaling amplifier, determines the full-scale range of the MAX1217/MAX1218/MAX1219. To compensate for gain errors or increase/decrease the ADC's full-scale range, the voltage of this bandgap reference can be indirectly adjusted by configuring JU1/JU2 and adjusting potentiometer R119/R120 on the MAX1217/MAX1218/MAX1219 EV kits. Connecting a potentiometer between REFADJ and REFIO increases the full-scale range of the ADC. Conversely, connecting the potentiometer between REFADJ and GND decreases

the full-scale range. The MAX1217/MAX1218/MAX1219 feature two sets of pins to calibrate each channel independently; thus, the MAX1217/MAX1218/MAX1219 EV kits feature two sets of reference circuitry. Jumper JU1 and potentiometer R119 control the reference of channel A. Jumper JU2 and potentiometer R120 control the reference of channel B. See Table 4 for shunt settings.

Table 4. Reference Shunt Settings (JU1, JU2)

SHUNT POSITION	DESCRIPTION
1-2	Internal reference disabled. Apply a reference voltage at the REFIO pad.
3-4*	Internal reference enabled.
5-6	REFADJ connected through potentiometer R119/R120 to REFIO.
7-8	REFADJ connected through potentiometer R119/R120 to GND.

**Default configuration: JU1 (3-4), JU2 (3-4).*

Output Signal

The MAX1217/MAX1218/MAX1219 feature two, parallel LVDS-compatible, digital output buses. Each output bus transmits the digitized analog input signals of channels A and B. An additional output (CLK) is provided for data synchronization. Refer to the MAX1217, MAX1218, MAX1219 data sheets for more details.

Output Format

The digital output coding can be set to either two's complement or straight offset binary by configuring jumper JU3 and JU4. Each channel can be set independently. Jumper JU3 controls the output format of channel A. Jumper JU4 controls the output format of channel B. See Table 5 for shunt positions.

Table 5. Output Format Shunt Settings (JU3, JU4)

SHUNT POSITION	$\overline{T}$/B PIN	DESCRIPTION
1-2	AVCC	Digital output in straight offset binary format.
2-3*	GND	Digital output in two's-complement format.

**Default configuration: JU3 (2-3), JU4 (2-3).*

Output Bit Locations

The digital outputs of the MAX1217/MAX1218/MAX1219 are connected to headers J8, J9, and J10. PC board trace lengths are matched to minimize data skew and improve the dynamic performance of the device. In addition, seven drivers (U3–U9) buffer and level-translate the ADC's digital outputs to LVPECL-compatible signals. The drivers increase the differential voltage swing, and are able to support large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to headers J11, J12, and J13. See Table 6 for bit location of headers J8–J13.

Table 6. Output Bit Locations (Differential Capture)

SIGNAL		CHANNEL A UNBUFFERED = J8 BUFFERED = J11	CHANNEL B UNBUFFERED = J10 BUFFERED = J13
OR	P	1	49
	N	2	50
D11	P	5	45
	N	6	46
D10	P	9	41
	N	10	42
D9	P	13	37
	N	14	38
D8	P	17	33
	N	18	34
D7	P	21	29
	N	22	30
D6	P	25	25
	N	26	26
D5	P	29	21
	N	30	22
D4	P	33	17
	N	34	18
D3	P	37	13
	N	38	14
D2	P	41	9
	N	42	10
D1	P	45	5
	N	46	6
D0	P	49	1
	N	50	2
SIGNAL		UNBUFFERED	BUFFERED
CLK	P	J9-3	J12-3
	N	J9-4	J12-4

P: True. *N: Complementary.*

Note: *Requires differential logic analyzer.*

Output Bit Locations (Single-Ended Capture)

The MAX1217/MAX1218/MAX1219 EV kits feature a third set of headers (J16, J17, J18) that allow a single-ended logic analyzer to capture the output data of the MAX1217/MAX1218/MAX1219. The single-ended outputs are buffered by U3–U9. The output data has a typical 2V common-mode voltage and a single-ended 750mV$_{P-P}$ voltage swing. For best results, adjust the logic analyzer's trigger threshold to the common-mode voltage. See Table 7 for single-ended bit locations.

Table 7. Output Bit Locations (Single-Ended Capture)

SIGNAL	CHANNEL A	CHANNEL B
	J16	J18
OR	1	73
D11	7	67
D10	13	61
D9	19	55
D8	25	49
D7	31	43
D6	37	37
D5	43	31
D4	49	25
D3	55	19
D2	61	13
D1	67	7
D0	73	1
SIGNAL	**CHANNEL A AND B**	
CLK	J17-4	

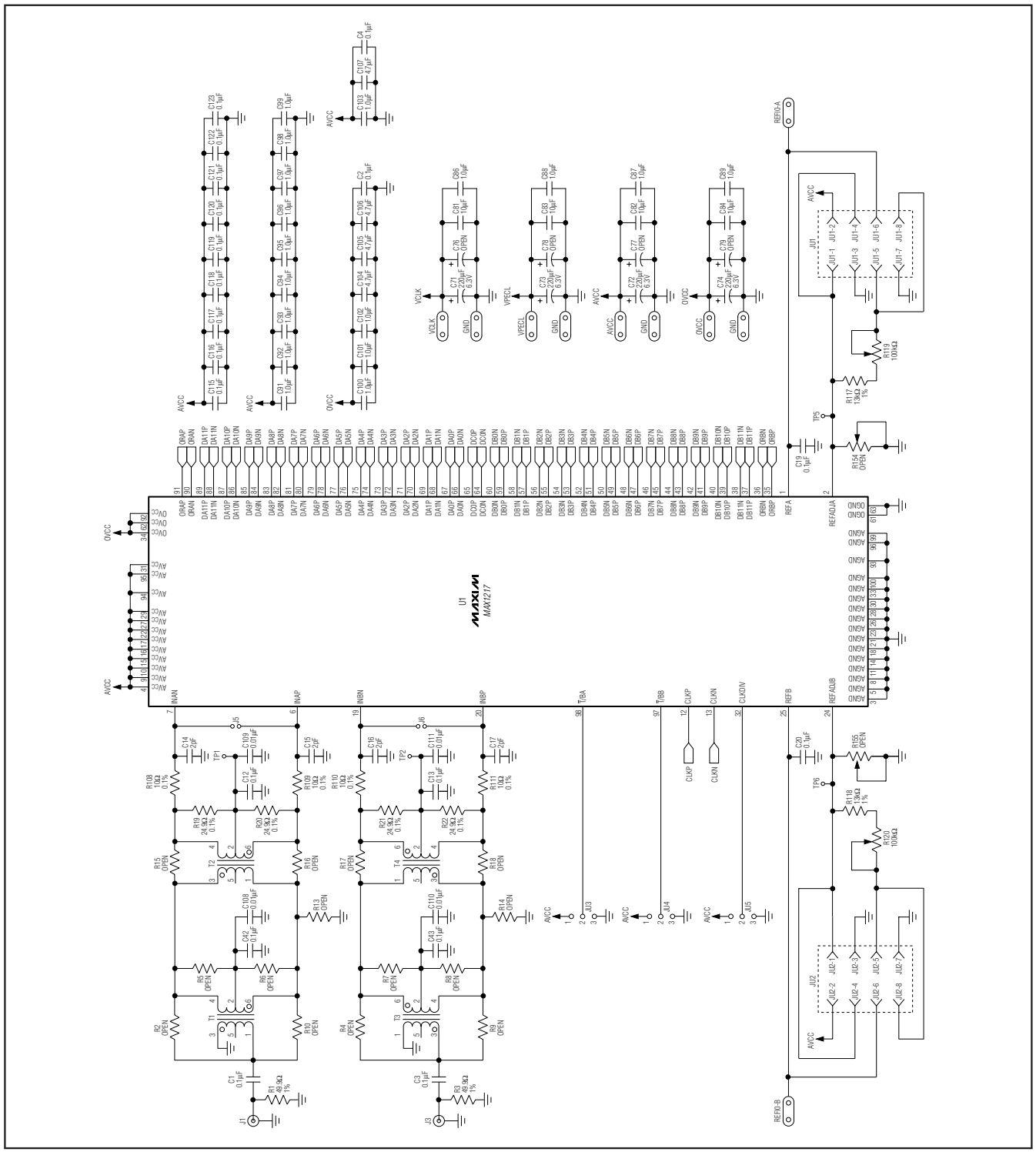

Figure 1a. MAX1217 EV Kit Schematic (Sheet 1 of 7)

MAX1217/MAX1218/MAX1219 Evaluation Kits

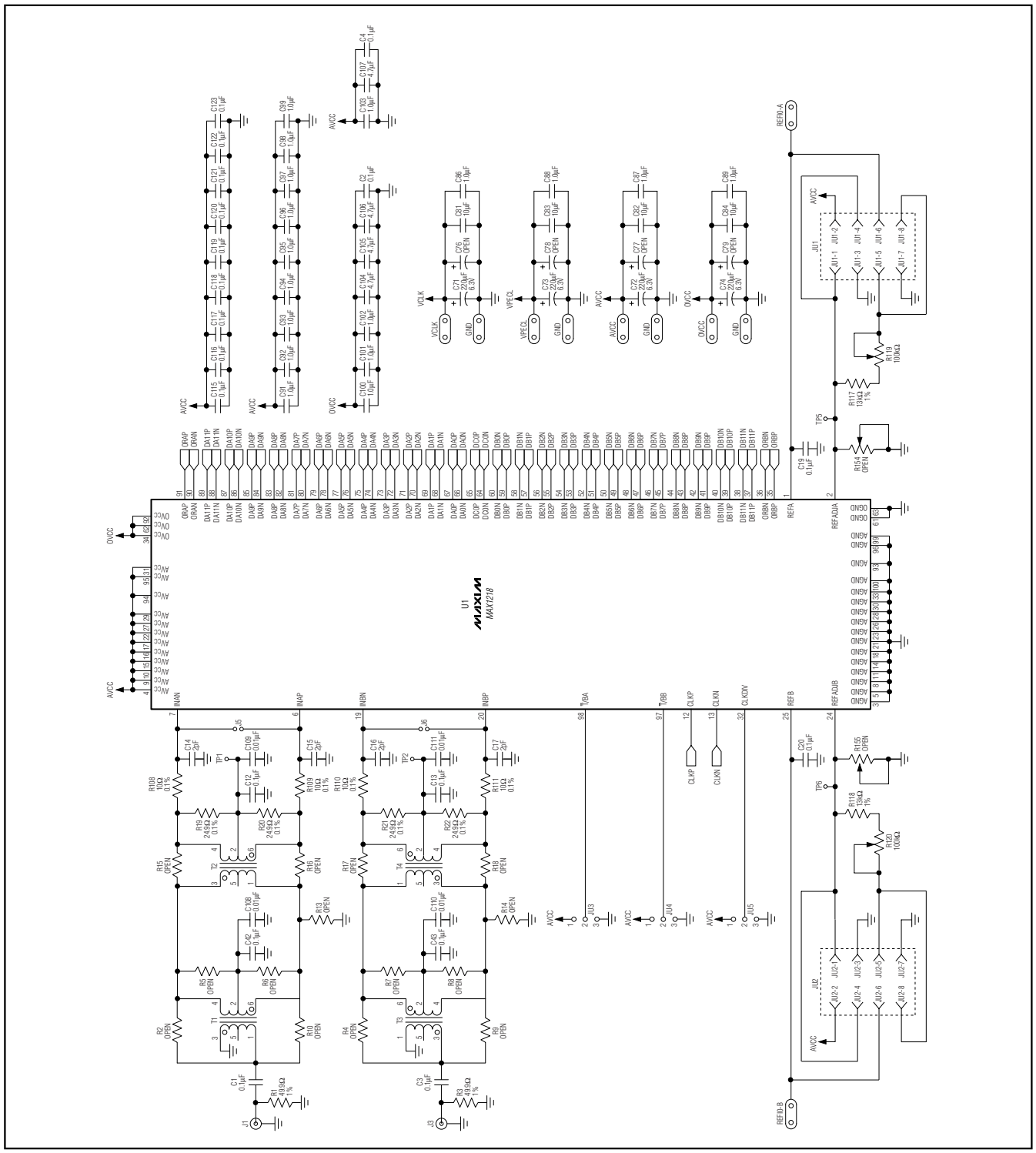

Figure 1b. MAX1218 EV Kit Schematic (Sheet 1 of 7)

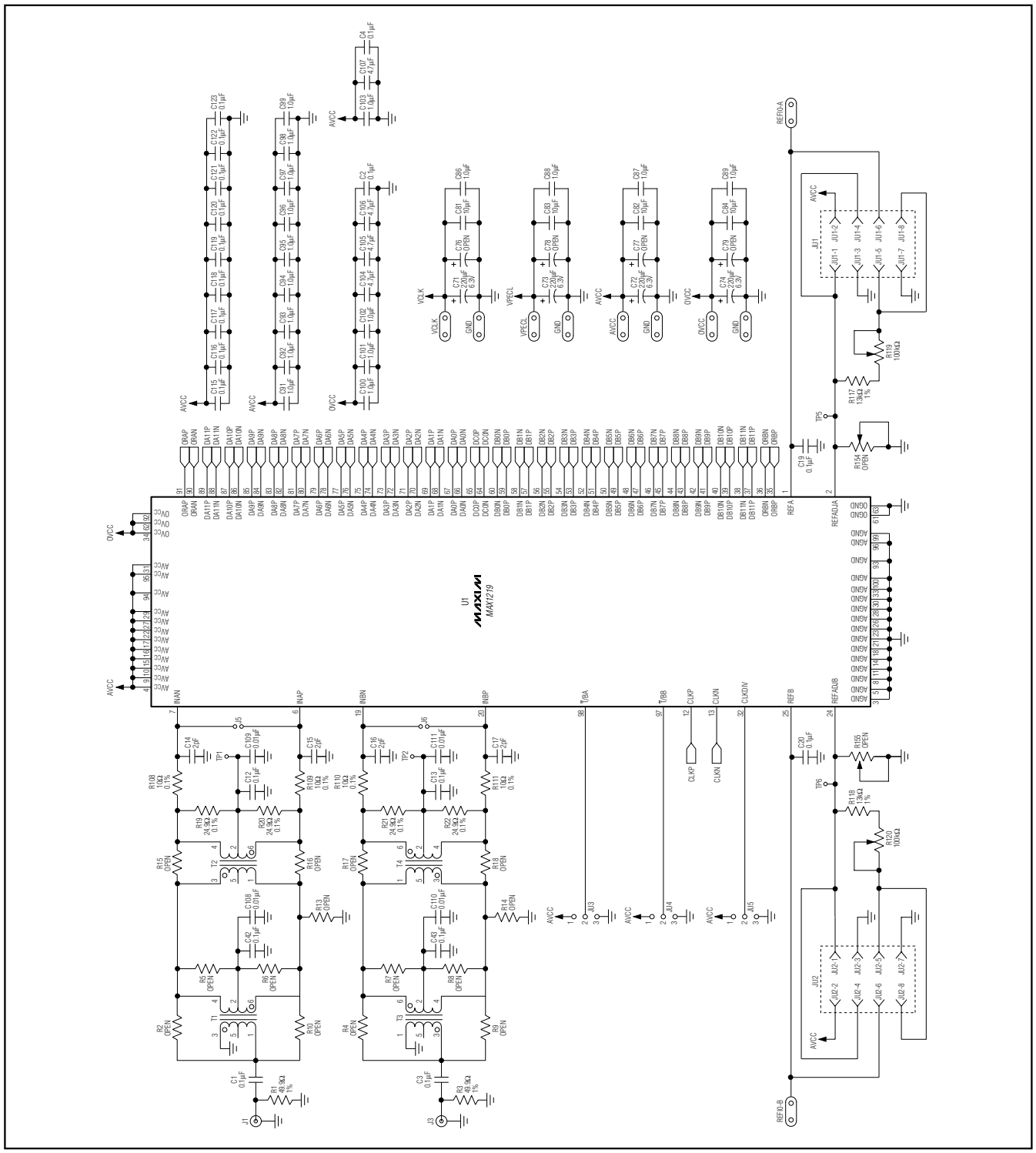

Figure 1c. MAX1219 EV Kit Schematic (Sheet 1 of 7)

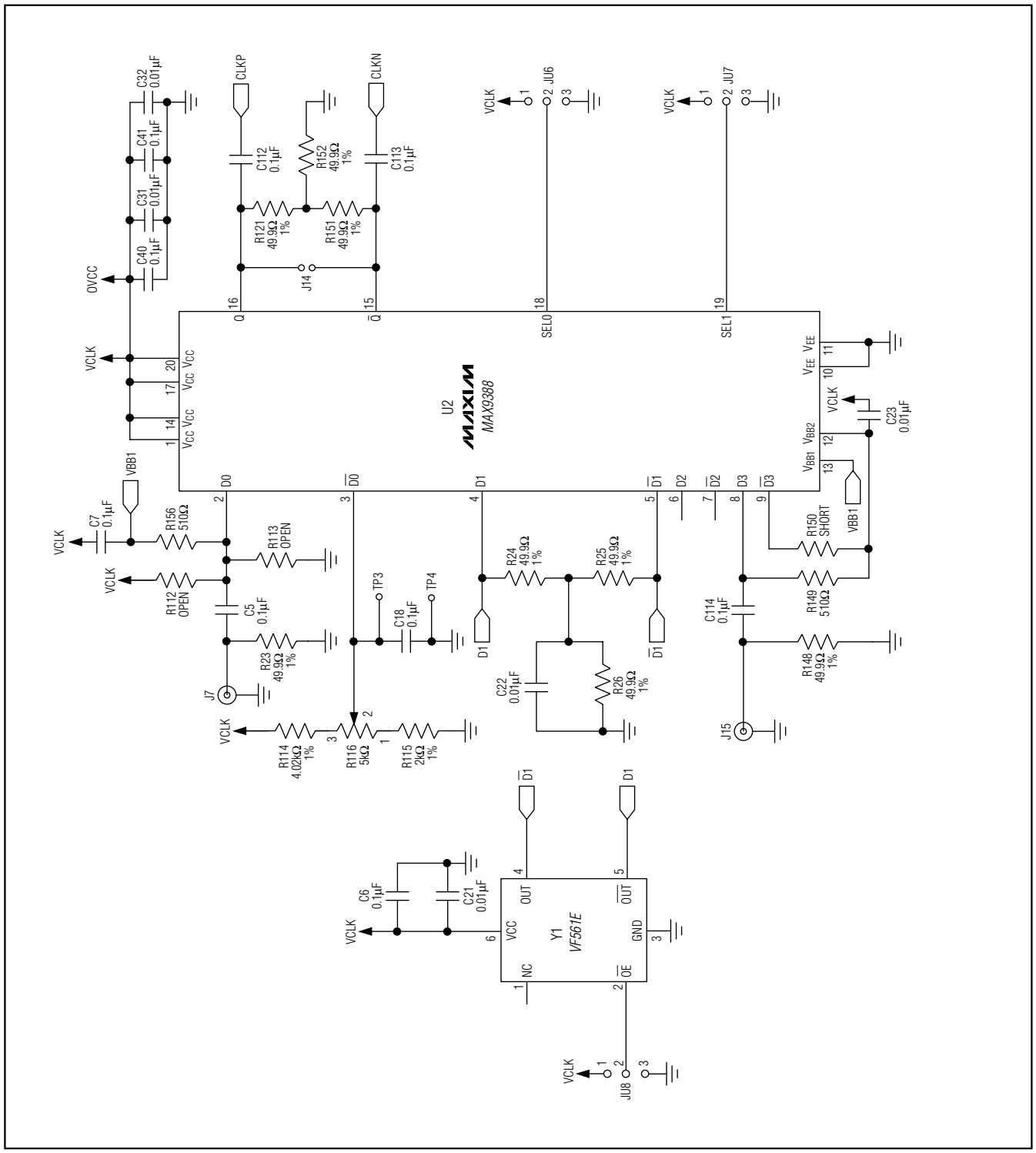

Figure 1d. MAX1217/MAX1218/MAX1219 EV Kit Schematic (Sheet 2 of 7)

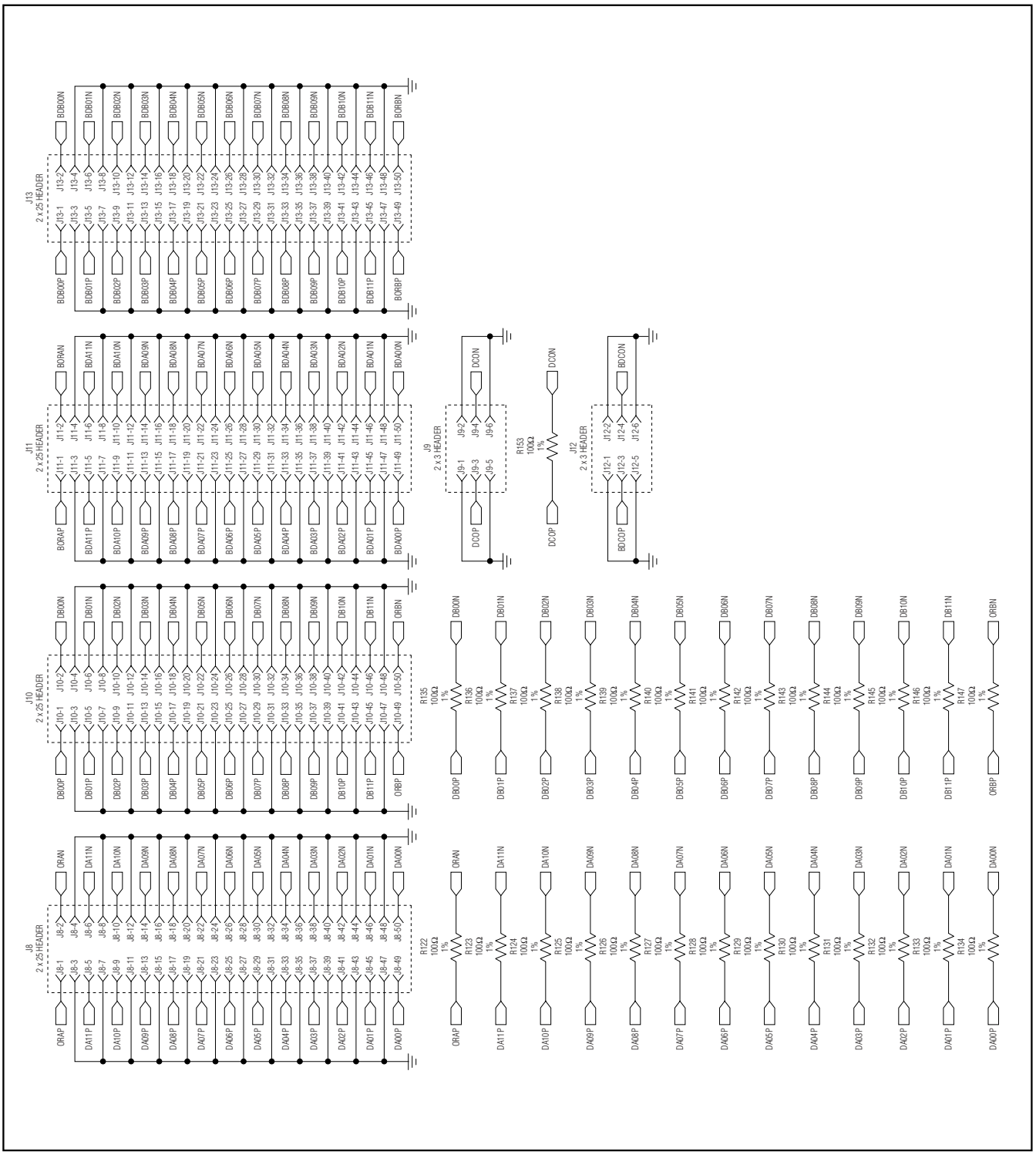

Figure 1e. MAX1217/MAX1218/MAX1219 EV Kit Schematic (Sheet 3 of 7)

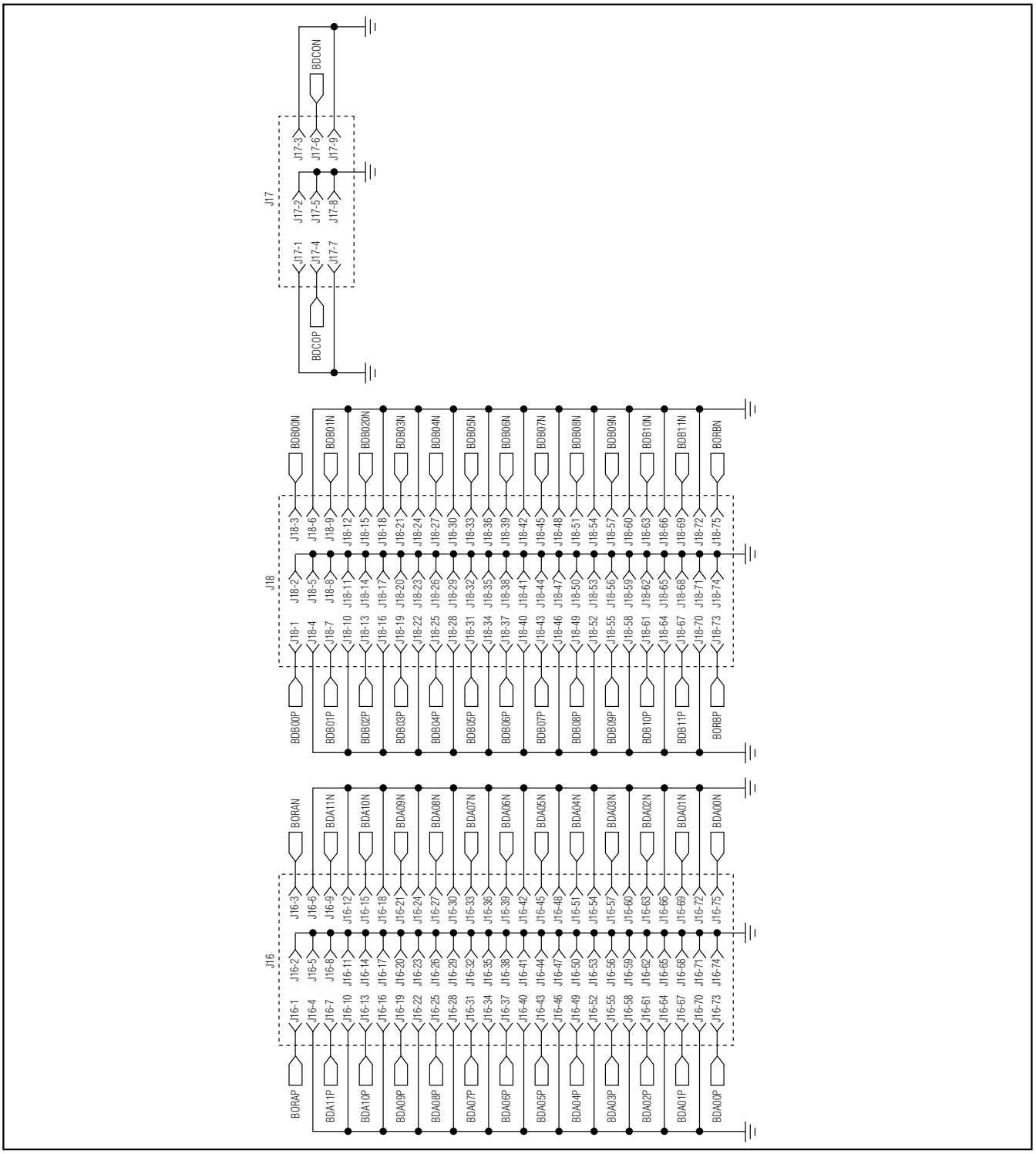

Figure 1f. MAX1217/MAX1218/MAX1219 EV Kit Schematic (Sheet 4 of 7)

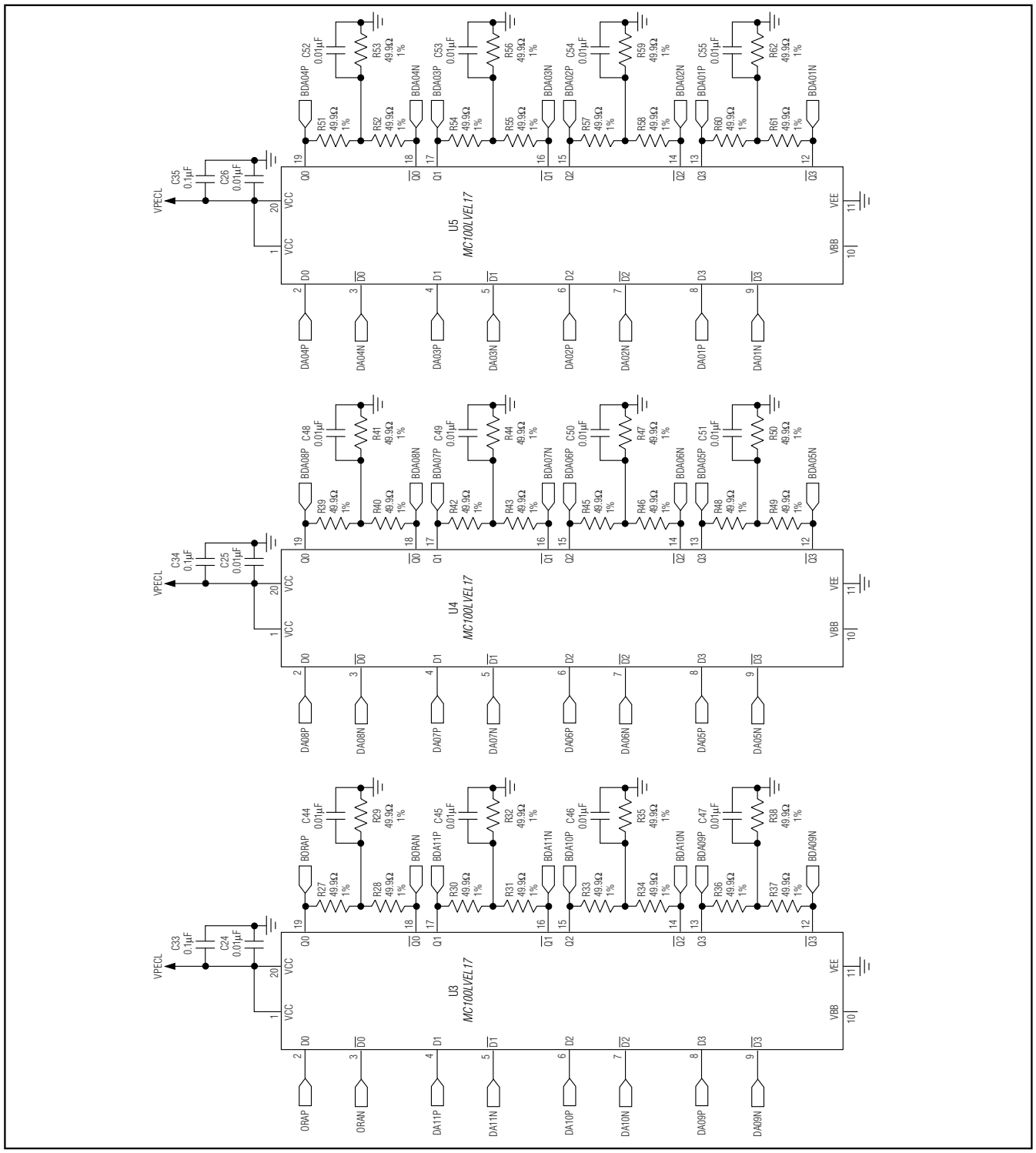

Figure 1g. MAX1217/MAX1218/MAX1219 EV Kit Schematic (Sheet 5 of 7)

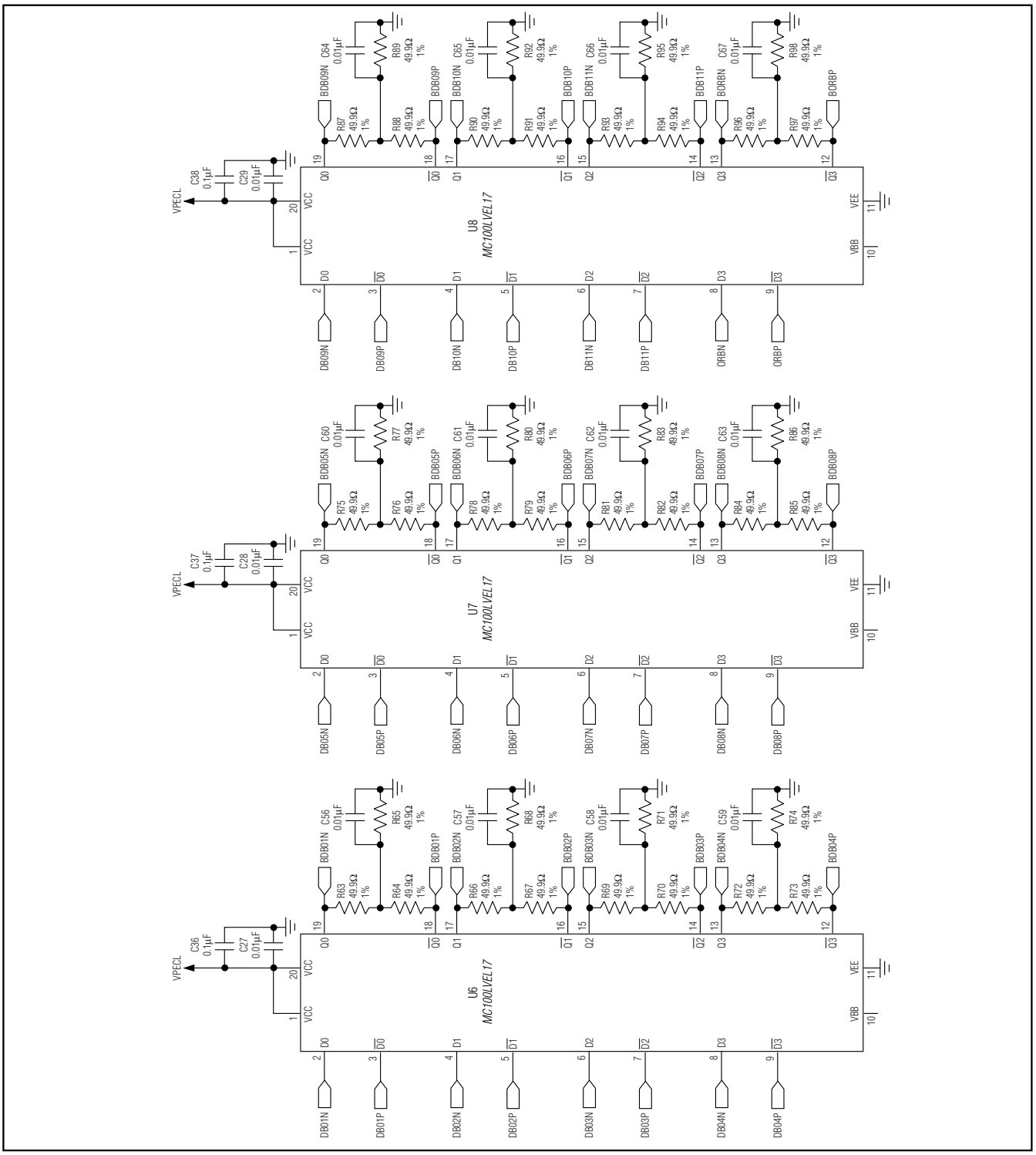

Figure 1h. MAX1217/MAX1218/MAX1219 EV Kit Schematic (Sheet 6 of 7)

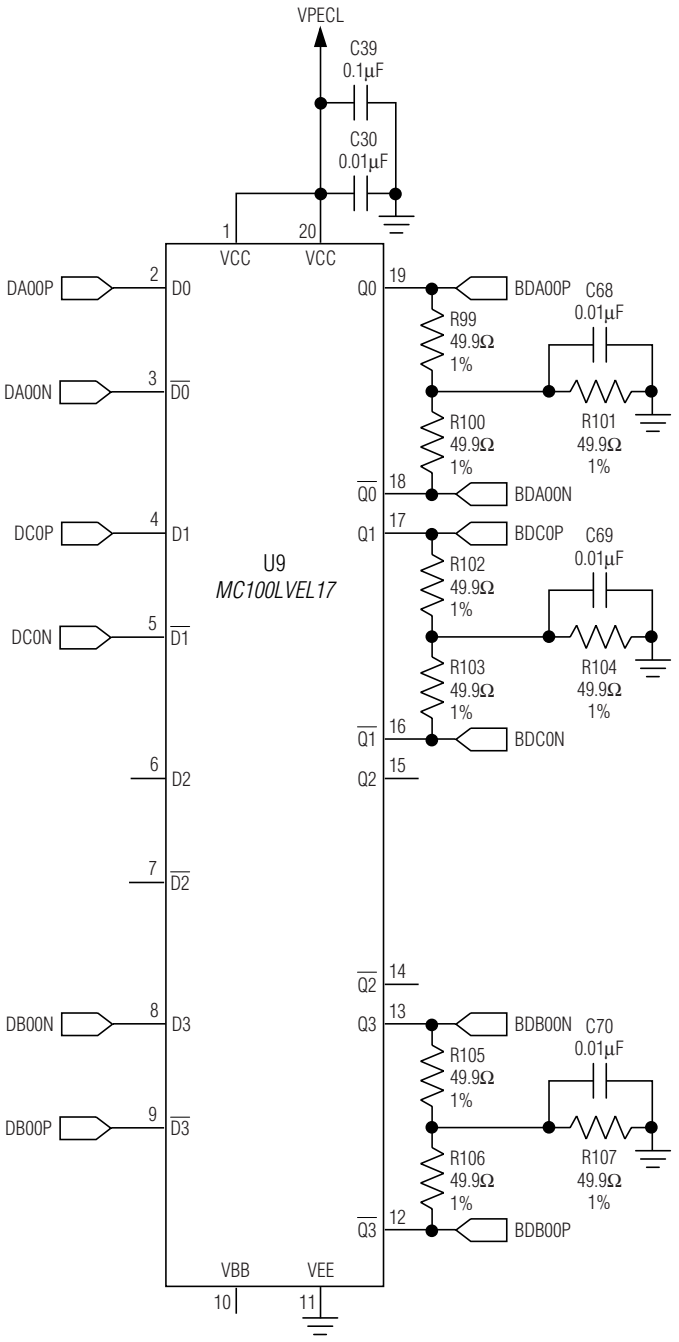

Figure 1i. MAX1217/MAX1218/MAX1219 EV Kit Schematic (Sheet 7 of 7)

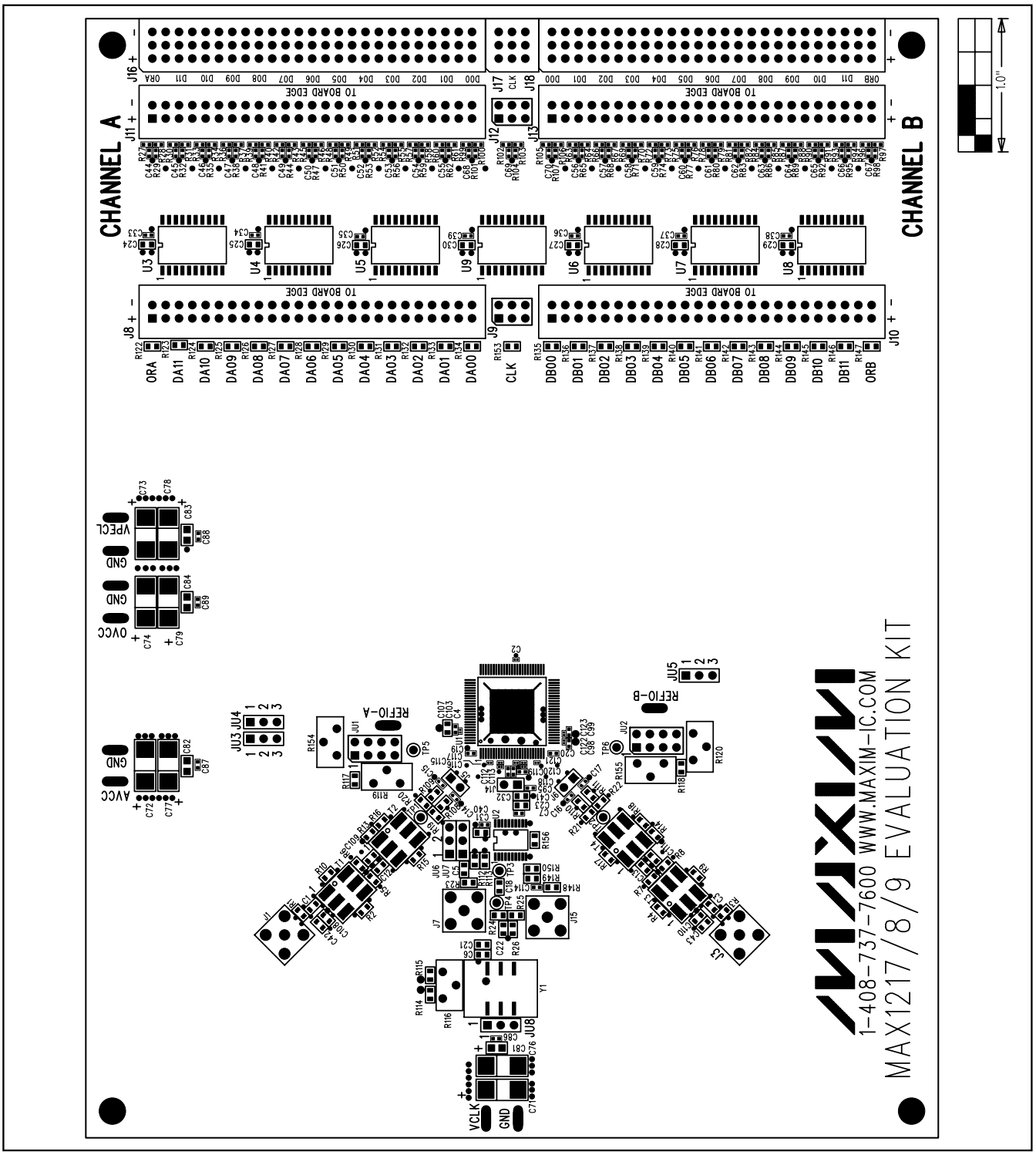

Figure 2. MAX1217/MAX1218/MAX1219 EV Kit Component Placement Guide—Component Side

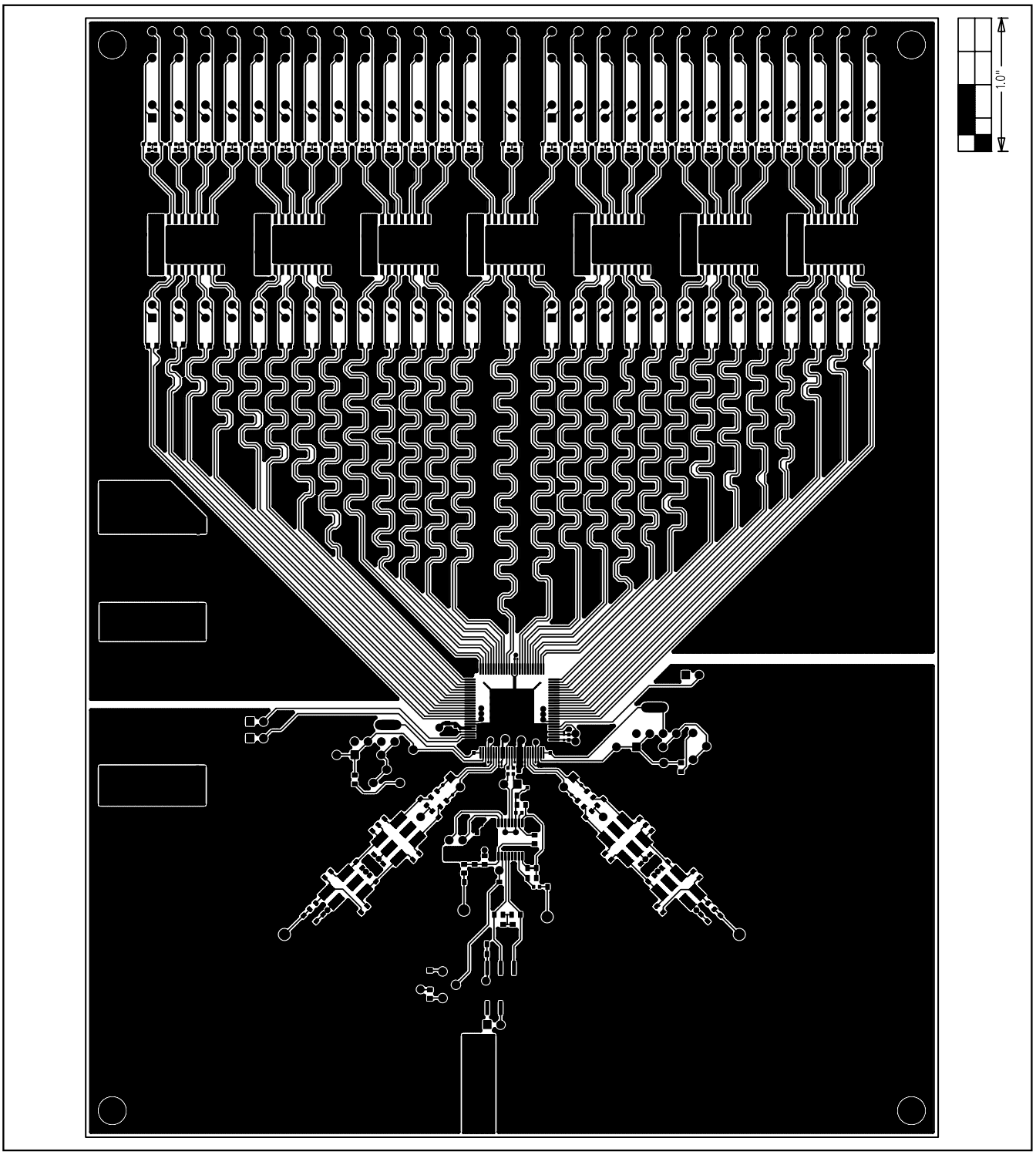

Figure 3. MAX1217/MAX1218/MAX1219 EV Kit PC Board Layout—Component Side

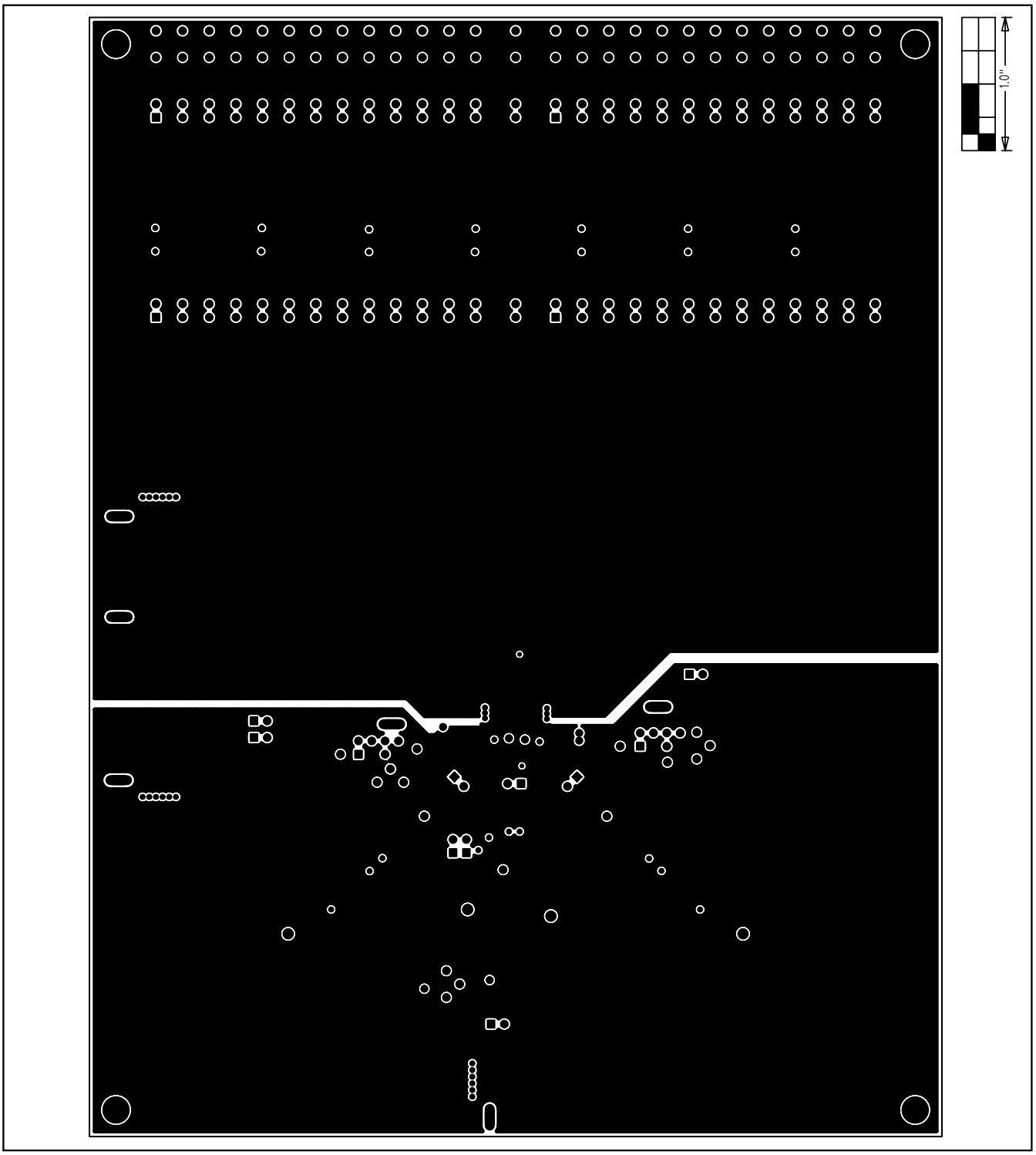

Figure 4. MAX1217/MAX1218/MAX1219 EV Kit PC Board Layout—Ground Planes

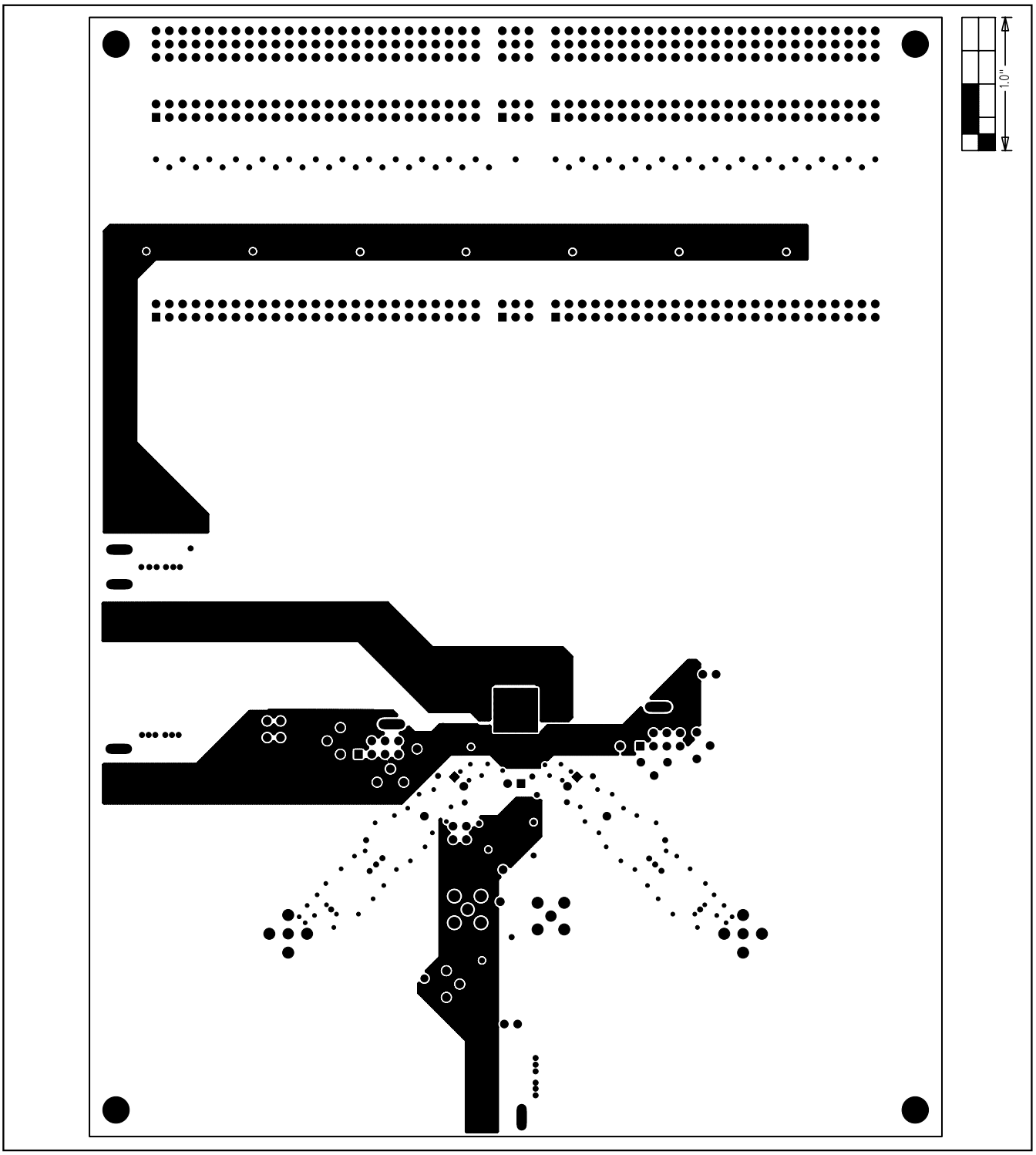

Figure 5. MAX1217/MAX1218/MAX1219 EV Kit PC Board Layout—Power Planes

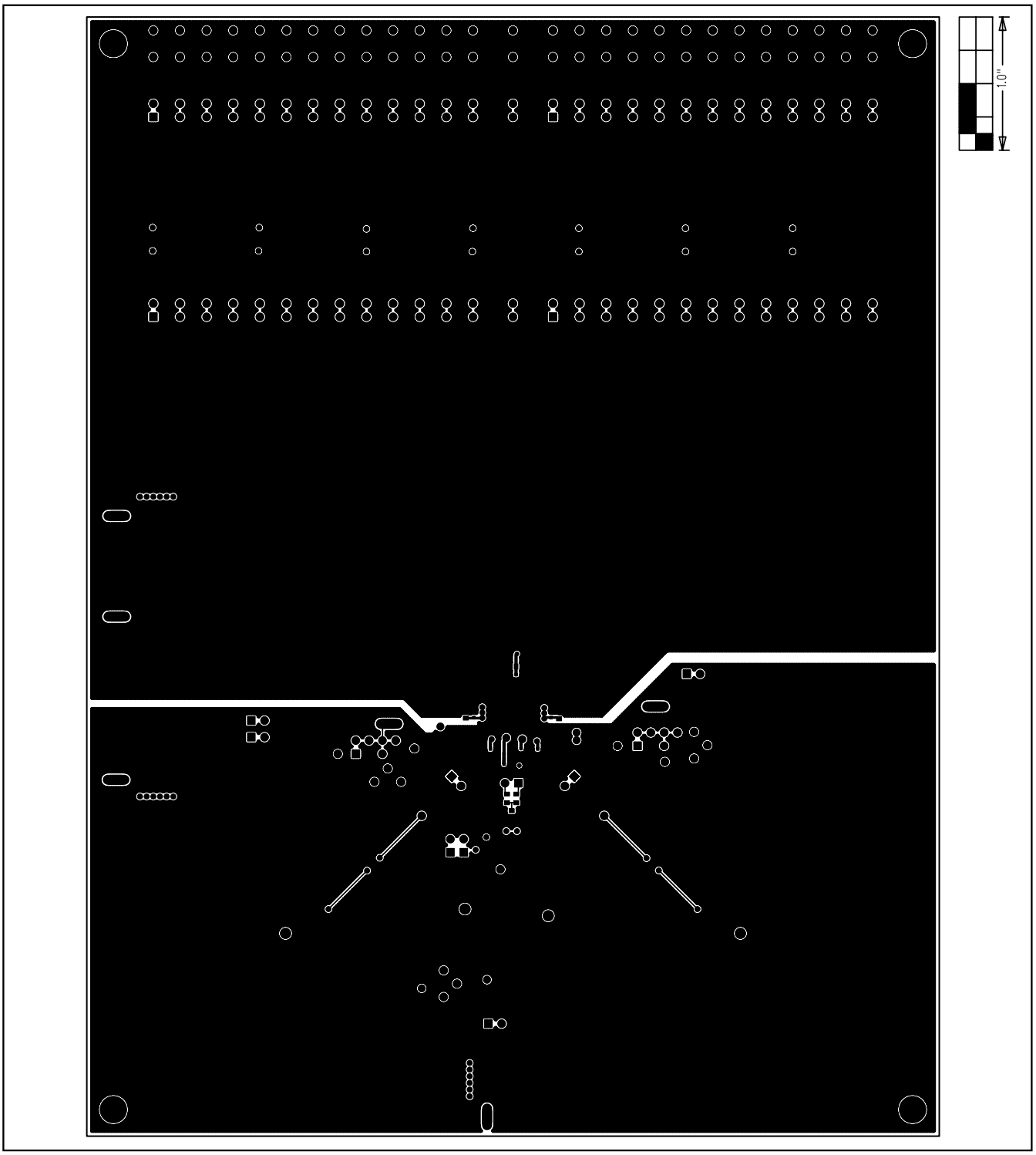

Figure 6. MAX1217/MAX1218/MAX1219 EV Kit PC Board Layout—Solder Side

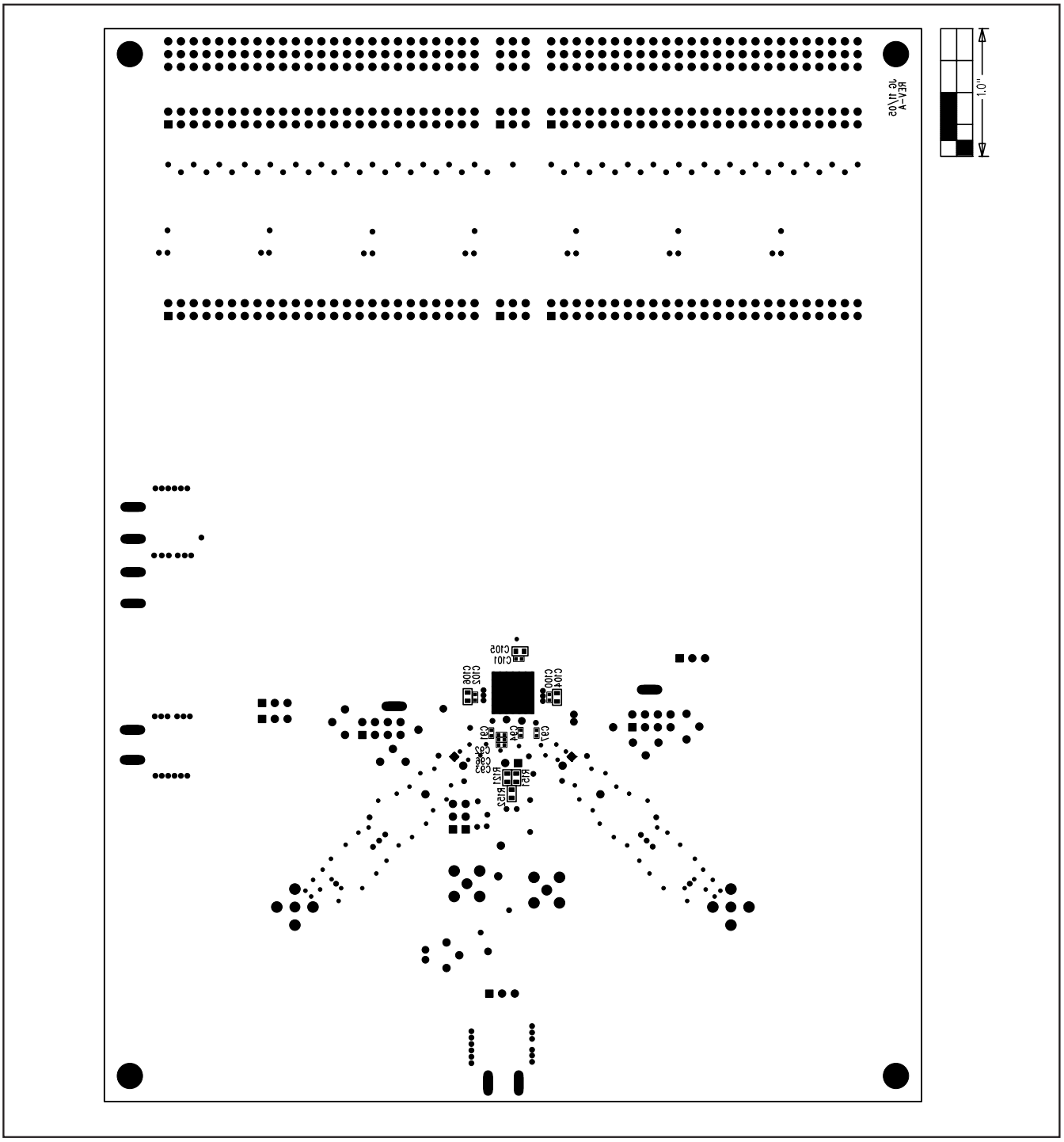

Figure 7. MAX1217/MAX1218/MAX1219 EV Kit Component Placement Guide—Solder Side